US-PAT-NO: 5105437

DOCUMENT-IDENTIFIER: US 5105437 A

TITLE: Programmable digital acquisition and tracking controller

DATE-ISSUED: April 14, 1992

US-CL-CURRENT: 375/149, 375/367 , 380/34

APPL-NO: 07/ 559013

DATE FILED: July 26, 1990

——— KWIC ———

Detailed Description Text - DETX (10):

Summing circuit 79 and accumulator 83 comprise a programmable signal level threshold detector adapted to produce a single bit decision output on line 85. This single bit decision is actually just the sign bit of accumulator 83. The sign bit transition on line 85 is produced when the data on line 82 causes the value in the preset accumulator 83 to change sign. The transition sign bit on line 85 is applied to the detector logic 86. Logic 86 is also monitoring the count zero that appears on line 87 after a predetermined time period that has been set in the sample time counter 88 from the programmable microprocessor on line 89. The programmable count set on line 89 is not counted by the bit strobe on line 91 until enabled by the signal on line 92 from the detector logic 86. The enable signal on line 92 is applied as a hold enable signal to the accumulator 83 which is loaded by the reset signal produced on line 93 from the detector logic 86. The signal on line 93 loads the value X in the accumulator 83 at the same time the value Y is loaded into the sample time counter 88. The hold signal on line 92 is only used during the acquisition mode and will now be explained in greater detail.

US-PAT-NO: 6510483

DOCUMENT-IDENTIFIER: US 6510483 B1

TITLE: Circuit, architecture and method for reading an address counter and/or matching a bus width through one or more synchronous ports

DATE-ISSUED: January 21, 2003

US-CL-CURRENT: 710/307, 365/189.02 , 365/230.02 , 710/51 , 710/52 , 711/211 , 713/600

APPL-NO: 09/ 531365

DATE FILED: March 21, 2000

PARENT-CASE:

CROSS REFERENCE TO RELATED APPLICATIONS

The present application may relate to co-pending application Ser. No. 09/531,341, filed concurrently, which is hereby incorporated by reference in its entirety.

——— KWIC ———

Claims Text - CLTX (6):

6. The apparatus according to claim 5, wherein said plurality of counter control signals is selected from the group consisting of (i) an address strobe signal, (ii) a counter enable signal, and (iii) a counter reset signal.

Claims Text - CLTX (19):

19. The method according to claim 18, wherein said plurality of counter control signals is selected from the group consisting of (i) an address strobe signal, (ii) a counter enable signal, and (iii) a counter reset signal.